CLAIMS

What is claimed is:

1. A chip scale package for connecting a flip chip die having alternating signal and ground connections to a primary circuit board, said chip scale package comprising:

a substrate comprising a top side for mounting the flip chip die and a bottom side for mounting said substrate to the primary circuit board;

a set of top-side pads on said top side of said substrate, respective ones of said top-side pads corresponding to respective ones of the substantially alternating signal and ground connections of the flip chip die;

a set of bottom-side pads on said bottom side of said substrate for electrically connecting with the primary circuit board, respective ones in said set of bottom-side pads corresponding to respective ones in said set of top-side pads; and

a plurality of conductive paths extending through said substrate from said top side to said bottom side and electrically coupling respective ones in said set of top-side pads to respective ones in said set of bottom-side pads, said conductive paths arranged to maintain alternating signal and ground connections between respective ones of said top-side pads and respective ones of said bottom-side pads.

2. The chip scale package of claim 1 wherein each one of said conductive paths comprises:

a via extending through said substrate from said top side to said bottom side;

a top-side trace coupling a corresponding one in said set of top-side pads to said via; and

a bottom-side trace coupling a corresponding one in said set of bottom-side pads to said via.

3. The chip scale package of claim 1 wherein said set of bottom-side pads comprises an inner array of bottom side pads and an outer array of bottom side pads, both said inner and outer arrays of bottom-side pads arranged as alternating signal and ground connection pads.

4. The chip scale package of claim 3 wherein said conductive paths comprise alternating signal and ground transmission lines between respective ones in said top-side set of pads and respective ones in said inner and outer sets of bottom-side pads.

5. The chip scale package of claim 1 wherein said substrate further comprises a top-side signal layer on said top side of said substrate, said set of top-side pads disposed on said top-side signal layer, and a bottom-side signal layer on said bottom side of said substrate, said set of bottom-side pads disposed on said bottom-side signal layer.

6. The chip scale package of claim 1 further comprising the flip chip die bonded to said top-side of said substrate.

7. The chip scale package of claim 6 further comprising underfill material sealing a bottom edge of the flip chip die.

8. The chip scale package of claim 1 further comprising:

a ground plane disposed on said bottom-side of said substrate within a central area of said bottom side of said substrate, said bottom side pads disposed generally about said ground plane;

a plurality of thermal solder balls coupled to said ground plane to electrically and thermally couple said ground plane with the primary circuit board;

a plurality of thermal vias projecting upward from said ground plane through said substrate to said top side of said substrate such that said plurality of thermal vias are beneath the flip chip die when the flip chip die is mounted to said top side; and

conductive traces coupling selected ones of said conductive paths that are connected to electrical ground to said thermal vias.

9. A chip scale package for connecting a flip chip die having signal and ground connections to a primary circuit board, said chip scale package comprising:

a substrate comprising a top side with a mounting area for receiving the flip chip die and a bottom side for connecting said substrate to the primary circuit board;

a first set of signal and ground pads on said top side of said substrate to electrically connect with the corresponding signal and ground connections on the flip chip die;

a second set of signal and ground pads on said bottom side of said substrate to electrically connect the flip chip die with the primary circuit board;

a plurality of signal and ground conductive paths extending from said top side to said bottom side of said substrate to electrically connect respective ones

of said first set of signal and ground pads with respective ones of said second set of signal and ground pads,

a ground plane on said bottom side of said substrate within a central area substantially beneath said mounting area of the flip chip die;

a plurality of grounded thermal vias extending upward through said substrate from said ground plane;

a plurality of conductive traces to connect selected ones of said ground conductive paths to respective ones of said grounded thermal vias to electrically connect said selected ones of said ground conductive paths to said ground plane; and

a plurality of thermal solder balls coupled to said ground plane to provide electrically and thermally conductive paths from said ground plane to the primary circuit board.

10. The chip scale package of claim 9 further comprising a second plurality of solder balls, respective ones of said second plurality of solder balls coupled to respective ones of said second set of signal and ground pads.

11. The chip scale package of claim 9 wherein said first set of signal and ground pads comprise a top-side rectangular array of spaced apart signal and ground pads in an alternating signal and ground pattern.

12. The chip scale package of claim 11 wherein said plurality of signal and ground conductive paths comprise alternating signal and ground conductive paths corresponding to the alternating signal and ground pattern of said top-side rectangular array of spaced apart signal and ground pads.

13. The chip scale package of claim 12 wherein each said signal conductive path and each said ground conductive path comprises:

a via extending through said substrate from said top side to said bottom side of said substrate;

a top-side conductive trace coupling a top end of said via to a respective one of said first set of signal and ground pads; and

a bottom-side conductive trace coupling a bottom end of said via to a respective one of said second set of signal and ground pads.

14. A chip scale package to couple a flip chip die having a set of signal and ground connections with a primary circuit board, said chip scale package comprising:

a substrate comprising top and bottom sides, said top side of said substrate having a mounting area for receiving the flip chip die;

a first set of pads on said top side of said substrate arranged in an alternating pattern of signal and ground pads to electrically connect with the set of signal and ground pads on the flip chip die;

a second set of pads on said bottom side of said substrate corresponding to said first set of pads, said second set of pads arranged in an alternating pattern of signal and ground pads;

a plurality of conductive paths extending through said substrate and interconnecting corresponding ones of said first and second sets of pads in an alternating signal and ground pattern;

a ground plane on said bottom side of said substrate in an area of said bottom side substantially opposite said mounting area on said top side;

a plurality of thermal vias extending upward from said ground plane into said mounting area on said top side of said substrate to provide low thermal impedance paths between the flip chip die and said ground plane; and

a plurality of thermal solder balls coupled to said ground plane to extend the low thermal impedance paths to the primary circuit board.

15. The chip scale package of claim 14 further comprising conductive traces coupling selected ones of said conductive paths to respective ones of said thermal vias to establish electrically conductive paths from the flip chip die to said ground plane.

16. The chip scale package of claim 14 wherein said second set of pads comprises:

an inner rectangular array of spaced apart signal and ground pads; and

an outer rectangular array of spaced apart signal and ground pads.

17. The chip scale package of claim 16 wherein said first set of pads comprises a rectangular array of spaced apart signal and ground pads.

18. The chip scale package of claim 17 wherein said plurality of conductive paths comprise alternating connections between successive ones of said rectangular array of spaced apart signal and ground pads in said first set of pads and respective ones of said inner and outer rectangular arrays of spaced apart signal and ground pads in said second set of pads.

19. The chip scale package of claim 14 further comprising a plurality of solder balls coupled to respective ones in said second set of signal and ground pads to couple said second set of signal and ground pads to the primary circuit board.

20. The chip scale package of claim 14 further comprising:

a top-side solder mask formed on a portion of said top side of said substrate; and

a bottom-side solder mask formed on a portion of said bottom side of said substrate.

21. The chip scale package of claim 14 further comprising the flip chip die mounted to said top side of said substrate.

22. The chip scale package of claim 21 further comprising an underfill epoxy sealing an interface between said flip chip die and said top side of said substrate.

23. The chip scale package of claim 14 wherein each said conductive path in said plurality of conductive paths comprises:

a via extending through said substrate from said top side to said bottom side;

a top-side conductive trace coupling one of said first set of signal and ground pads to said via; and

a bottom-side conductive trace coupling the corresponding one of said second set of signal and ground pads to said via.

24. The chip scale package of claim 23 wherein said via comprises a plated-through-hole in said substrate.

25. A chip scale package for a flip chip die having a set of signal and ground connections, said chip scale package comprising comprising:

a substrate comprising top and bottom sides, said top side of said substrate comprising a mounting area to receive the die;

a first array of alternating ground and signal pads disposed on said top side of said substrate to electrically connect with corresponding ones in the set of signal and ground connections on the die;

a second array of alternating ground and signal pads disposed on said bottom side of said substrate corresponding to said first array, said pads in said second array adapted to carry solder balls for attaching said substrate to a primary circuit board;

a central ground plane disposed on said bottom side of said substrate and positioned substantially opposite said mounting area on said top side of said substrate;

a first plurality of vias for electrically connecting said pads on said top side with said pads on said bottom side, respective ones of said first and second arrays of pads coupled to said vias by conductive traces on said respective top and bottom sides of said substrate;

a second plurality of vias positioned within said mounting area on said top side of substrate, and extending from said top side into said central ground plane on said bottom side to provide thermal conduction paths between the die and said central ground plane; and

a plurality of thermal solder balls coupled to said central ground plan to provide thermal and electrical connections between said central ground plane and the primary circuit board.

26. The chip scale package of claim 25 wherein said conductive traces coupling respective ones of said first and second arrays of pads to said first plurality of vias comprise alternating signal and ground conductors arranged such that substantially all signal-carrying ones of said conductive traces are separated by intervening ground-carrying ones of said conductive traces.

27. The chip scale package of claim 25 wherein said central ground plane comprises a solid copper plane centrally positioned on said bottom side of said substrate.

28. The chip scale package of claim 25 wherein said thermal solder balls comprise solder balls directly coupled to said central ground plane.

29. The chip scale package of claim 25 wherein said first array of alternating ground and signal pads on said top side of said substrate comprises a peripheral array of interleaved ground and signal bump pads to mate with corresponding solder bumps on the die.

30. The chip scale package of claim 29 wherein said first plurality of vias comprise:

an outer set of vias arranged about an outer perimeter of said peripheral array of interleaved signal and ground bump pads; and

an inner set of vias arranged about an inner perimeter of said peripheral array of interleaved signal and ground bump pads.

31. The chip scale package of claim 30 wherein said conductive traces comprise:

top-side conductive traces on said top side of said substrate to couple individual ones in said peripheral array of interleaved signal and ground bump pads

to corresponding ones in said inner and outer sets of vias comprising said first plurality of vias; and

bottom-side conductive traces on said bottom side of said substrate to couple individual ones in said second array of alternating ground and signal pads to corresponding ones in said inner and outer sets of vias comprising said first plurality of vias;

said top-side and bottom-side conductive traces preserving said signal and ground interleaving to minimize trace-to-trace coupling between signal-carrying ones of said conductive traces.

32. The chip scale package of claim 25 wherein said substrate comprises a five-millimeter square chip carrier.

33. A carrier for interconnecting a flip chip with a primary circuit board comprising:

an array of ground and signal conductive paths extending through the carrier for grounding the flip chip and directing signals from the flip chip to the primary circuit board; and wherein the ground conductive paths are interposed between the signal conductive paths so as to generally isolate the signal conductive paths from each other.

34. The carrier of claim 33 wherein the carrier includes a central area and wherein the array of ground and signal conductive paths are disposed generally around the central area.

35. The carrier of claim 33 wherein consecutive ground and signal conductive paths are offset with respect to each other.

36. The carrier of claim 33 wherein each conductive path includes a via connected between a pair of generally horizontally disposed conductive traces disposed on opposite sides of the carrier.

37. The carrier of claim 33 wherein each conductive path includes a first terminal end disposed on one side of the carrier and a second terminal end disposed on the other side of the carrier; and wherein the first terminal ends of the conductive paths lie in a single row that extends generally around the one side of the carrier while the second terminal ends lie in two generally parallel rows that extend generally around the other side of the carrier.

38. The carrier of claim 37 wherein consecutive second terminal ends of the conductive paths are staggered along the two rows.

39. A carrier for interconnecting a flip chip with a primary circuit board and managing the transfer of heat generated by the flip chip, comprising:

a) least one thermal via formed in the carrier for transferring heat originating from the flip chip;

b) a ground plane contacting the at least one thermal via for permitting heat to be transferred from the thermal via to the ground plane; and

c) at east one conductor associated with the ground plane for transferring heat from the ground plate to the primary circuit board.